AMENDMENT TO THE CLAIMS

Please amend the claims as follows:

1.(Original) A method of adding a plurality of partial products, wherein each partial product has a plurality of bits having respective binary weights, wherein each bit can have a first or second logic state, the method comprising:

forming a first set of multiple-bit columns from bits of the plurality of partial products, wherein the bits in each column of the first set have the same binary weight; and

encoding each multiple-bit column in the first set into a respective modified partial product, which represents a number of bits in the column having the first logic state.

2.(Original) The method of claim 1 and further comprising:

forming a second set of multiple-bit columns from bits of the modified partial products, wherein the bits bit in each column of the second set have the same binary weight as one another; and

encoding each column in the second set into a respective further modified partial product, which represents a number of bits in the column having the first logic state.

3.(Original) The method of claim 1 and further comprising:

repeating the steps of forming and encoding to form successive sets of further modified partial products until the number of further modified partial products is reduced to a desired number.

5.(Original) The method of claim 3 and further comprising:

adding the desired number of further modified partial products to produce a product.

6.(Original) The method of claim 1 wherein encoding comprises:

for each multiple-bit column in the first set, forming a modified column word by packing all the bits in that column having the first logic state into a first contiguous set of bit positions in the modified column word; and

generating the respective modified partial product based on a pattern of the first and second logic states in the modified column word.

7.(Original) The method of claim 6 wherein:

forming a modified column word comprises packing all the bits in that column having the first logic state to one end of the modified column word; and

generating comprises generating the respective modified partial product based on the bit positions in the modified column word at which values of the bits in the modified column word transition between the first and second logic states.

8.(Original) The method of claim 6 wherein the modified column word comprises first and second opposite ends and the step of forming the modified column word comprises, for each multiple-bit column in the first set:

(a) grouping adjacent ones of the bits of the multiple-bit column into a present level of multiple-bit groups;

(b) for each group in the present level, packing any of the bits in that group having the first logic state toward a first end of that group, which corresponds in orientation to the first end of the modified column

word, to form a respective modified present level group;

(c) grouping adjacent ones of the modified present level groups into respective higher level groups, with the higher level groups becoming the present level groups;

(d) repeating step (b) for the present level groups generated in step (c); and

(e) repeating steps (b) through (d) until there is only one present level group, which has the same number of bit positions as the modified column word and any of the bits in that group having the first logic state have been packed toward the first end of that group.

9.(Original) The method of claim 8 wherein step (b) comprises shifting the bits in that group having the first logic state to different bit positions in that group through a multiplexer.

10.(Original) A method of multiplying a multiplicand by a multiplier, the method comprising:

generating a plurality of partial products, wherein each partial product has a plurality of bits having respective binary weights, wherein each bit can have a first or second logic state;

forming a first set of multiple-bit columns from bits of the plurality of partial products, wherein the bits in each column of the first set have the same binary weight; and

encoding each multiple-bit column in the first set into a respective modified partial product, which represents a number of bits in the column having the first logic state.

11.(Original) The method of claim 10 and further comprising:

forming a second set of multiple-bit columns from bits of the modified partial products, wherein the bits bit in each column of the second set have the same binary weight as one another; and

encoding each column in the second set into a respective further modified partial product, which represents a number of bits in the column having the first logic state.

12.(Original) The method of claim 11 and further comprising:

repeating the steps of forming and encoding to form successive sets of further modified partial products until the number of further modified partial products is reduced to a desired number.

13.(Original) The method of claim 12 and further comprising:

adding the desired number of further modified partial products to produce a product.

14.(Original) The method of claim 10 wherein encoding comprises:

for each multiple-bit column in the first set, forming a modified column word by packing all the bits in that column having the first logic state into a first contiguous set of bit positions in the modified column word; and

generating the respective modified partial product based on a pattern of the first and second logic states in the modified column word.

15.(Original) The method of claim 14 wherein:

forming a modified column word comprises packing all the bits in that column having the first logic state to one end of the modified column word; and

generating comprises generating the respective modified partial product based on the bit positions in the modified column word at which values of the bits in the modified column word transition between the first and second logic states.

16.(Currently Amended) The method of claim 14 wherein the modified column word comprises first and second opposite ends and the step of forming the modified column word comprises, for each multiple-bit column in the first set:

(a) grouping ~~adjacent ones~~ one or more of the bits of the multiple-bit column that are adjacent to one another into a present level of multiple-bit groups;

(b) for each group in the present level, packing any of the bits in that group having the first logic state toward a first end of that group, which corresponds in orientation to the first end of the modified column word, to form a respective modified present level group;

(c) grouping ~~adjacent ones~~ one or more of the modified present level groups that are adjacent to one another into respective higher level groups, with the higher level groups becoming the present level groups;

(d) repeating step (b) for the present level groups generated in step (c); and

(e) repeating steps (b) through (d) until there is only one present level group, which has the same number of bit positions as the modified column word and any of the bits in that group having the first logic state have been packed toward the first end of that group.

17.(Original) The method of claim 16 wherein step (b) comprises shifting the bits in that group having the first logic state to

different bit positions in that group through a multiplexer.

18.(Original) The method of claim 10 wherein generating a plurality of partial products comprises, for each partial product:

multiplexing the multiplicand multiplied by zero, the multiplicand multiplied by one, the multiplicand multiplied by minus one, the multiplicand multiplied by two, and the multiplicand multiplied by minus two to produce the respective partial product.

19.(Original) A multiplier circuit comprising:

a partial products generator comprising a multiplicand input, a multiplier input and a plurality of partial product outputs, wherein each output has a plurality of bits having respective binary weights and which can have a first or second logic state; and

adding means for forming a first set of multiple-bit columns from bits of the plurality of partial product outputs, wherein the bits in each column of the first set have the same binary weight, and encoding each column in the first set into a respective modified partial product, which represents a number of bits in the column having the first logic state.

20.(Original) The multiplier circuit of claim 19 wherein the partial products generator comprises a plurality of multiplexers, wherein each multiplexer multiplexes the multiplicand multiplied by zero, the multiplicand multiplied by one, the multiplicand multiplied by minus one, the multiplicand multiplied by two, and the multiplicand multiplied by minus two to a respective one of the partial product outputs.

21.(Original) The multiplier circuit of claim 19 wherein the adding means comprises:

means for forming a second set of multiple-bit columns from bits of the modified partial products, wherein the bits bit in each column of the second set have the same binary weight as one another; and

encoding means for encoding each column in the second set into a respective further modified partial product, which represents a number of bits in the column having the first logic state.

22.(Original) The multiplier circuit of claim 21 wherein the adder means further comprises:

means for repeating the steps of forming and encoding to form successive sets of further modified partial products until the number of further modified partial products is reduced to a desired number.

23.(Original) The multiplier circuit of claim 19 wherein the adding means comprises:

packing means for each multiple-bit column in the first set, for forming a modified column word by packing all the bits in that column having the first logic state into a first contiguous set of bit positions in the modified column word; and

generating means for generating the respective modified partial product based on a pattern of the first and second logic states in the modified column word.

24.(Original) The multiplier circuit of claim 23 wherein:

the packing means comprises means for packing all the bits in that column having the first logic state to one end of the modified column word; and

the generating means comprises means for generating the respective modified partial product based on the bit positions in the modified column word at which values of the bits in the modified column word transition between the first and second logic states.

25.(New) The method of claim 1 and further comprising:

receiving an accumulation feedback value and using the accumulation feedback value as an additional member of the plurality of partial products in the steps of forming and encoding.

26.(New) The method of claim 25 wherein the step of receiving an accumulation feedback value comprises receiving a plurality of feedback values and using the plurality of feedback values as additional members of the plurality of partial products in the steps of forming and encoding.

27.(New) The method of claim 10 and further comprising:

receiving an accumulation feedback value and using the accumulation feedback value as an additional member of the plurality of partial products in the steps of forming and encoding.

28.(New) The method of claim 27 wherein the step of receiving an accumulation feedback value comprises receiving a plurality of feedback values and using the plurality of feedback values as additional members of the plurality of partial products in the steps of forming and encoding.

29.(New) The multiplier circuit of claim 19 and further comprising:

an accumulation feedback input, which feeds an accumulation

value back to the adding means such that the adding means uses the accumulation value as an additional member of the plurality of partial products.

30.(New) The multiplier of claim 29 wherein the accumulation feedback input comprises first and second accumulation feedback inputs for receiving first and second feedback values, respectively, which are used by the adder means as additional members of the plurality of partial products.